ICM

LANS-100

S-100 BUS

LOCAL AREA

NETWORK CONTROLLER

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**** INTRODUCTION ****

Microprocessor based networks have evolved predominantly into two catagories: BUS STRUCTURED NETWORKS & LOCAL AREA NETWORKS. INTERCONTINENTAL MICRO SYSTEMS (ICM) has established itself as a frontrunner in bus structured networks by combining the S100 Bus, ICM's state-of-the-art S100 BUS Memory Mapped/DMA Slave Processors (CPS series), the CPZ4800X Single Board Central Processor (SBCP) and Software 2000's powerful TurboDOS(tm) as the Software Operating System. Bus structured networks have proven to be very cost effective with high performance for office environments requiring up to sixteen users. If, however, a greater number of users are required and the advantages of bus structred networks such as file sharing, record & file locking and peripheral sharing are to be maintained, Local Area Networking (LAN) has proven to be the appropriate technique. Networking 255 Master Processors with up to 16 slaves each allows one to build a sophisticated 4000 user system with true filesharing and record locking.

ICM will provide you, our valued customer, with the hardware and software tools required to interlink bus networks through a powerful MODIFIED TOKEN PASSING communications protocol refered to as ARCnet (tm). ICM has carefully evaluated the alternatives and finds that Token Passing Networking is the clear choice over Carrier-Sensing Multiple Access/Collision Detection (CSMA/CD) Networking such as ETHERNET (tm). Token Passing has a clearcut price/performance ratio advantage. ETHERNET based hardware is typically three times more expensive than TOKEN PASSING hardware.

ICM proudly announces the LANS100 Local Area Network Controller which is an S100 Bus controller (IEEE 696.1/D2) providing Modified Token Passing local area networking capability between S100 Bus systems, workstations and other computing systems incorporating the same networking technique and ARCnet protocol.

The LANS100, ICM's TurboLAN(tm) software package, and CPZ-4800X SBCP (acting as a host), constitute a high performance, high throughput network node (application processor). A powerful network file server may be implemented by adding Floppy drives, a Hard-disk controller & Hard-disk drives, printers and other peripherals to this node. The systems integrator can network up to 255 nodes. Each node may consist of a bus structured network, PC's or other intelligent workstations.

FEATURES

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* IEEE 696.1/D2 S100 Bus Compliance.
* I/O Polled or Interrupt Driven via VI Lines.
* Compatible with the CPZ 4800X SBCP, any 8 bit CPU (with or without extended address compatibility) or any 16 bit CPU complying with IEEE 696.1/D2 Bus specification.
* Provides Interface from S100 Bus System to S100Bus System or from S100 Bus Systemto Workstation viaaModified Token Passing ARCnet Protocol Network.
* LAN Data Rate of 2.5 Megabits/Second.
* Attachment of up to 255 Nodes per Network Segment.
*Network self configures as nodes are added or deleted from network.
* Network efficiency increases with increasing attachment of nodes.
* Compatible with any interconnect media such as coaxial cable (RG62/93 ohm), twisted pair, etc.
* Up to 40 miles between nodes with use of repeaters (HUBS).
* 16 bit CRC check & generation.
* No host processor overhead for link control.
* TurboDOS Operating System compatible.

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PERFORMANCE SPECIFICATIONS
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Bus Interface.................................IEEE 696.1/D2 S100
       Status, control, data & address. I/O port addressjumper
       selectable for address range from 00h toFFh.Message
       Buffer address jumper selectable for address range from
       010000h to FFFFFFh.
              Phantom.....Requires connection if Message Packet
                     Buffer resides within first 64Kbyte of
                     System Memory. Not required with CPZ-
                     4800X if used in Map mode.
              Ready.......Requires connection to XRDY or PRDY
                     for synchronous access to Data Packet
                     Buffer and control registers.
              Interrupt...Interupts Host Processor when status
                     bits become stable. Interrupt connected
                     via one of 8 VI lines.

Network Interface.......Modified Token Passing Local Area Network
       Transmission Mode..................................Baseband
       Transmission Medium...........Coaxial Cable/RG62(93 ohm)
       Transmission Distance.....................2000 feet (max)
       Transmission Speed.......................2.5 Mbps, Typical
       Transmission Voltage
              Transmit Mode...................20.1V P-P Typical
              Receive Mode.....................6.7V P-P Typical
       Protocol...ARCnet

Data Packet Buffer.....................2 Kbyte X 8 Bit Static RAM
       Wait states...........Requires connection to XRDY or PRDY
              for synchronous access to Data Packet Buffer
       Direct memory transfers............to/from CPZ-4800X SBCP
              Data transfer rate (non-DMA).......190 Kbytes/sec
              Data transfer rate (DMA)...........571 Kbytes/sec
       Memory address...................switch selectable in 64
              Kbyte boundries.

Power Requirements
       Voltages...............................+8 VDC @ 1.0 A(max)
                                              -16 VDC @ 25 MA(max)
       Power...8.5 W(max)

Operating Environment
       Temperature......................0 to 45 Degrees Celsius
       Relative Humidity..................................0 to 95%

Construction
       Circuit Board...................Double Sided Glass Epoxy,
              Vacrel Solder over Bare Copper.
       All IC's in Sockets
       TESTING...........Completely tested and 24 hour burned-in
       WARRANTY.............One Year Warranty (Parts and Labor)

**** FUNCTIONAL DESCRIPTION ****

The LANS100 is functionally partitioned into the following major groups:

   --Local Area Network Driver(LAND)/Interface

   --local Area Network Controller(LANC)

   --LANC ID Logic

   --Data Packet Buffer

   --Wait State Generator

   --Memory Address Select Logic

   --I/O Port Address Select Logic

   --S100 Bus Interface

   Each group is described below to give the user a clear understanding of the hardware and software setup options. Prior to describing each group, a "thumbnail sketch" of the overall function of the LANS100 is first described.

In order to help conceptualize Token Passing Network systems the following terminology is given:

- RIM (Resource Interface Module):

A RIM is a microprocessor based controller which controls the data transmission, buffer management, error detection and system reconfiguration as other RIMS are added or deleted to the network. A processor requires a RIM to get on the network. The LANS100 is a RIM.

- HUB

A HUB is a repeater (amplifier) which extends the distance (range) between RIMS on the network. A PASSIVE HUB limits interconnect lengths to 2300 feet. An ACTIVE HUB can extend the range to 40 miles. A passive HUB can consist of up to 4 ports. The active HUB can be obtained in 8 or 16 port versions.

- FILE PROCESSOR

A File Processor (FP) is the processor which performs all major storage and data retrieval for the network. The File Processor:
> . Buffers data
> . Services data requests
> . Optimizes use of shared disk resources
> . Coordinates database transactions

A typical FP consists of a CPZ4800X SBCP, a hard disk controller, a tape controller and a RIM.

- APPLICATION PROCESSOR

The Application Processor (AP) is the processor which actually performs the user application programs. The application processor may be equipped with local storage, printers and other I/O devices. A typical AP could be a BUS STRUCTURED NETWORK consisting of a CPZ4800X SBCP, peripheral controllers, CPS series slave processors and a RIM. It could also be a PC with LAN capability or an intelligent terminal (workstation) with LAN capability.

A Local Area Network(LAN) typically consists of a file processor with several application processors interconnected via RIMS and one or more active HUBs. The interconnection media is normally coaxial cable. In ICM's case, the communications protocol of choice is the ARCnet Modified Token Passing protocol.

In a Token Passing arrangement, each RIM connected to the network is given an identification address. Next, a token (a unique 8-bit pattern such as 11111111) is sent to the first RIM (node). This token gives that node access to the network for transmitting purposes only. Node receivers are always on line. The node possessing the token sends a message by loading the ID of the intended receiver and the data packet to be transmitted in a data packet buffer. A command is then issued to transmit the ID and message packet followed by a 16 bit Cyclic Redundancy Check Character (CRC). If the intended receiver's ID matches with the transmitted ID, reception may then take place.

Each receiving node is responsible for acknowledging receipt of the token to prevent its loss. The node must respond in less than 78.2 microseconds; otherwise, the node is considered inoperative. The transferring node retains the token and a search is made for a node capable of receiving it. In this way, the network is never down, and a node can be removed without disrupting the network. An interrupt is generated by the transmitting node when sucessful delivery of the packet is accomplished.

After the message is sent, the token is passed to the next node in line. However, it need not be the node with the next identification address. Let's say that node 19 has possession of the token. It may pass that token to node 53 if so programmed. If node 53 has a message to send, it takes advantage of the token and uses the network. If it doesn't, it simply forwards the token to the next programmed node, and the token travels from node to node, giving each one a chance to use the network.

Local Area Network Driver(LAND)/Interface

The LANS100 utilizes a hybrid LAND which consists of passive and active components required to convert digital signals to dipulse format and vice versa and to transmit dipulse signals over coaxial cable, twisted pair or fiber optics. NRZ data is input to the LAND with data periods consisting of 400 ns intervals. Dipulses of 200 ns intervals are generated from this data and coupled to the coaxial cable via an RF transformer. In the same manner, dipulses being received are coupled into the LAND via the RF transformer. The LAND converts the dipulses into NRZ format.

The interface from the LAND is accomplished via a short coaxial cable with a Molex connector on one end and an RG62 connector at the other end. This cable is intended to connect the LANS100 to the rear of the typical S100 Bus chassis where RG62 cutouts are normally made. Coaxial cable may then be used to connect the chassis to the network.

Local Area Network Controller(LANC)

The LANC consists of the COM9026 special purpose communications adapter. The LANC contains a microprogrammed sequencer and logic necessary to effect the token passing mechanism of the network and to transceive data packets over that network. The LANC also reads a switch settable identification code which is used for node identification purposes. A switch setting is input to a shift register and the LANC reads the contents of the shift register during reset time. The LANC also controls data and address buffer transfers and Data Packet Buffer reads or writes. The host processor may read status or issue commands via I/O port cycles(IORQ). The host processor may read or write data from/to the Data Packet Buffer via memory cycles (MREQ). The Data Packet Buffer is also under control of the COM9026.

Data Packet Buffer

The Data Packet Buffer consists of a 2 Kbyte static RAM used to buffer up to four data packets with a maximun length of 508 bytes per message. The Data Packet Buffer is accessed by both the LANC and the host processor.

Wait State Generator

The COM9026 generates wait states to the host processor when the host processor executes either memory or I/O request cycles (MREQ or IORQ respectively). Because these access cycles run asynchronously with respect to the COM9026, the COM9026 places the host in wait states. The user has the option of generating the wait states either through XRDY or PRDY by selecting the wait generator source to the appropriate S100 Bus pin (jumper- READY SELECT).

LANC ID Logic

The LANC reads in a jumper settable identification code used for node identification purposes. A jumper setting is input to a shift register and the LANC reads the contents of the shift register during reset time. The jumper is identified on the board as LANC ID.

Memory Address Select Logic

The address bus consists of 24 lines designated as A0 through A23. During master memory access cycles in extended address mode, the address lines A0 through A10 address one of 2 Kbytes of the Data Packet Buffer. Address lines A11 through A23 map the Data Packet Buffer onto the master's address space. During master memory access cycles in PHANTOM MODE, the address lines A0 through A10 address one of 2 Kbytes of the Data Packet Buffer. Address lines A11 through A15 map the Data Packet Bufer onto the master's address space. However, PHANTOM is activated so that the master's system memory does not conflict with the Data Packet Buffer.

When the master executes a memory access cycle in extended address mode, a comparator on the LANS100 is enabled. It compares the master's extended address lines A16(m) through A22(m) against an eight position jumper referred to as the EXTND ADDR jumper. The remaining mapped address lines A11 through A15 are compared against the ONBOARD ADDR jumper. The EXTND ADDR jumper is sampled only if the ENABLE EXTN ADDR jumper is installed. If phantom operation is desired, the ENABLE EXTN ADDR jumper is not installed. Only the ONBOARD ADDR jumper is configured to specify the system's address space in which the Data Packet Buffer is to appear. Thus, A11 through A15 are compared against the ONBOARD ADDR jumper. The jumper PHANTOM must also be installed.

I/O Port Address Select Logic

Address lines A0 through A7 are used by the LANS100 during master I/O cycles to transfer I/O commands from the master and status inputs to the master.

The I/O Port Address Decoder consists of an eight bit comparator which compares the master's least significant address bits A0 through A7 against an eight position jumper referred to as the IOPORT ADDR jumper. If the master executes an I/O cycle transfer to the bus, and if the IOPORT ADDR jumper compares, the LANS100 will respond to either a master's command or to the master's request for the LANS100's status.

S100 BUS INTERFACE

The LANS100 S100-BUS interface consists of 69 lines. These are grouped into sets used to transmit data, control & power. The groups are:

Group	No. of lines
Address Bus	24
Input Data Bus	8
Output Data Bus	8
Status Bus	4
Control Input Bus	3
Vectored Interrupt Bus	8
Utility Bus	6
System Power	8

Devices connected on the bus are classified as either bus masters or bus slaves and as either permanent or temporary masters. The LANS100 is a bus slave. It cannot take control of the bus. Data transfers to/from the LANS100 are accomplished via memory-to-memory transfers from/to the master. Software may be configured to execute the transfers under DMA control in which case the transfer rate is approximately 571 Kbyte/second. Status and control are transfered through I/O port transfers from/to the master.

Each of the S-100 Bus signals utilized by the LANS100 are described on the following pages.

ADDRESS BUS

The address bus consists of 24 lines designated as A0 through A23. During master memory access cycles in extended address mode, the address lines A0 through A10 address one of 2 Kbytes of the Data Packet Buffer whereby address lines A11 through A23 map the Data Packet Buffer onto the master's address space. During master memory access cycles in PHANTOM MODE, the address lines A0 through A10 address one of 2 Kbytes of the Data Packet Buffer whereby address lines A11 through A15 map the Data Packet Bufer onto the master's address space. PHANTOM is activated so that the master's system memory does not conflict with the Data Packet Buffer.

Address lines A0 through A7 are used by the LANS100 during master I/0 cycles to transfer I/0 commands from the master and status inputs to the master.

INPUT DATA BUS

The input data bus consists of 8 lines designated as D00 through D07. Data inputs from the master are accepted during master memory & I/0 output cycles when the LANS100 is addressed appropriately.

OUTPUT DATA BUS

The output data bus consists of 8 lines desiginated as DI0 through DI7. Data outputs from the LANS100 to the master are accepted during master memory & I/0 input cycles when the LANS100 is addressed appropriately.

STATUS BUS

The status bus consists of 4 master output lines which define the current master processor bus cycle. The status lines used by the LANS100 are:

STATUS	FUNCTION
sMEMR	Master memory read cycle
sWO*	Master write cycle
sINP	Master input cycle
sOUT	Master output cycle

-sMEMR
     sMEMR is used by the LANS100 to generate memory read cycles.

-sWO*
     sWO* is used by the LANS100 to generate I/O and memory write
cycles in the LANC controller.

-sINP
     sINP is used to extract the LANS100's status:

```
BIT 7 6 5 4 3 2 1 0
    | | | | | | | |
    | | | | | | | +-----(RI) Receiver Inhibited
    | | | | | | |
    | | | | | | +-------(ETS2) Extended Timeout Status 2
    | | | | | |
    | | | | | +---------(ETS1) Extended Timeout Status 1
    | | | | |
    | | | | +-----------(POR) Power On Reset
    | | | |
    | | | +-------------(TEST) Test
    | | |
    | | +---------------(RECON) Reconfiguration
    | |
    | +-----------------(TMA) Transmit Message Acknowledged
    |
    +-------------------(TA) Transmitter Available
```
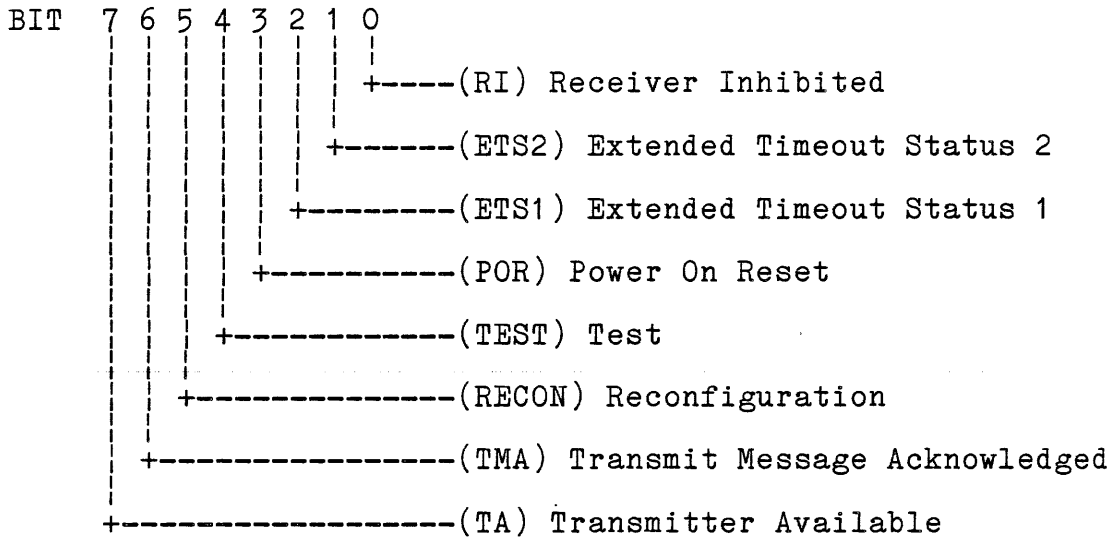

-sOUT
     sOUT is used in the LANS100 to execute one of the eight
commands to the LANS100:

```
BIT 7 6 5 4 3 2 1 0
    | | | | | | | |
    0 0 0 0 0 0 0 0   Reserved For Future Use
    0 0 0 0 0 0 0 1   Disable Transmitter
    0 0 0 0 0 0 1 0   Disable Receiver
    0 0 0 n n 0 1 1   Enable Transmit from Page nn
    b 0 0 n n 1 0 0   Enable Receive to Page nn;
                         Broadcast if b=1
    0 0 0 0 c 1 0 1   Define Configuration; c defines
                         Data Packet Buffer(DPB) Size;
                         c=1 DPB=2K; c=0 DPB=1K
    0 0 0 r p 1 1 0   Clear Flags; p=1 clears POR
                         status; r=1 clears RECON status
```

CONTROL INPUT BUS

The control input bus consists of 3 master output lines which define the master's current processor cycle. These consist of:

Signal	Function
pDBIN	Master read cycle
pWR*	Master write cycle
pSYNC	Master processor start cycle

-pDBIN

pDBIN is used in combination with the LANC's data request signal REQ to extract read data from the LANS100 to the S100 Bus.

-pWR*

pWR* is used to write input commands/data from the master to the LANS100.

-pSYNC

pSYNC is used to generate the appropriate wait generation timing to the master during I/O and memory cycles executed in the LANS100. It is also used in the LANC to latch the master's address during I/O and memory cycles.

VECTORED INTERRUPT BUS

The LANS100 may generate an interrupt to the master via the vectored interrupt bus. The interrupt pulse is generated by the LANC when certain status bits go active and corresponding register bit positions in the MASK register are set true. See MASK register bit assignments below. The user may connect the interrupt pulse generator to one of the eight vectored interrupt lines (VIO - VI7) through a jumper option. See "Solder/Trace Cut Options - VIX".

```
BIT  7 6 5 4 3 2 1 0
     | | | | | | | |
     | | | | | | | +-----Transmitter Available
     | | | | | | |
     | | | | | | +-------(not assigned)
     | | | | | |
     | | | | | +---------Recon Timer
     | | | | |
     | +-+-+-+-----------(not assigned)
     |
     +-------------------Receive Inhibit
```
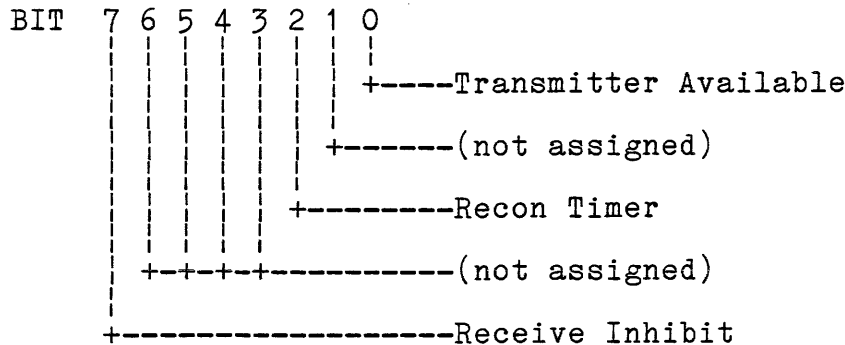
UTILITY BUS

The utility bus signals utilized by the slave consist of:

ϕ (Clock)	Master system clock
SIXTN*	Eight/Sixteendatatransfer status
RESET*	System Reset
SLVCLEAR*	Slave Clear
POC*	Power On Clear

-ϕ (Clock)
     ϕ is used in the LANS100 to generate the appropriate timing
for the wait state generator during the master's I/O or memory
cycle.

-SIXTN*
     This line is connected to a pull-up resistor via a jumper
option. If the master requires the Eight/Sixteen Data Transfer
Status to know the manner in which data transfers can be executed
on the S100 Bus, the sampling of this line by the master will
cause the master to do eight bit transfers only.

-RESET*/SLVCLR*/POC*
     The LANS100's reset line is asserted to clear the LANC
and other internal logic. One of three reset sources from the
master cause the LANS100 reset line to be asserted. The
selection of these reset siggnals is done via jumper option RESET
SELECT. The reset signals are:

     - Reset
     The master may issue a reset signal by asserting the bus
     reset signal RESET (S100 Bus pin 75).

     - Slave Clear
     The master may issue a reset signal by asserting the bus
     reset signal SLVCLR (S100 Bus pin 54).

     - Power-On Clear
     The master may issue a reset signal by asserting the bus
     reset signal POC (S100 Bus pin 99).

SYSTEM POWER

The system power utilized by the LANS100 consists of:

+8 to 10 VDC   (2 lines)
-16 to -21 VDC   (1 line)
           Ground   (5 lines)

The +8 VDC is input to a +5 VDC regulator to generate the power required by the LAND and the remaining logic. The - 16 VDC line is input to a -12 VDC regulator to generate the power required by the LAND. S100 Bus ground pins 20, 50, 53, 70 and 100 are connected to the PCB ground plane.

**** OPERATING INSTRUCTIONS ****

Instructions are given herein to configure the LANS100 from both the hardware and software standpoint.

Hardware Setup Instructions

The hardware is configured via jumper options and solder/trace cut areas. All jumper options and solder/trace cut areas are referred to by name on the silk screen of the PCB. The solder/trace cut options are located on the "solder" side of the board. Jumper areas are provided on the "component" side. These are implemented by header jumpers.

Jumper Options

Refer to figure 1 to locate the header jumper areas. These are designated as:

    EXTND ADDR
    ONBOARD ADDR
    ENABLE EXTN ADDR
    IOPORT ADDR
    LANC ID
    RESET SELECT
    READY SELECT

EXTENDED ADDRESS SELECT (EXTND ADDR)

The address bus consists of 24 lines designated as A0 through A23. During master memory access cycles in extended address mode, the address lines A0 through A10 address one of 2 Kbytes of the Data Packet Buffer whereby address lines A11 through A23 map the Data Packet Buffer onto the master's address address space. When the master executes a memory access cycle in extended address mode, a comparator on the LANS100 is enabled which compares the master's extended address lines A16 through A23 against the eight position EXTND ADDR jumper. The remaining mapped address lines A11 through A15 are compared against the ONBOARD ADDR jumper. The EXTND ADDR jumper is sampled only if the ENABLE EXTN ADDR jumper is installed.

```
                         EXTND ADDR

                       +------+
            (A23)  1   | 0  0 |  16
                       | 0  0 |
                       | 0  0 |
                       | 0  0 |
                       | 0  0 |
                       | 0  0 |
                       | 0  0 |
            (A16)  8   | 0  0 |  9
                       +------+
                         a  b
```
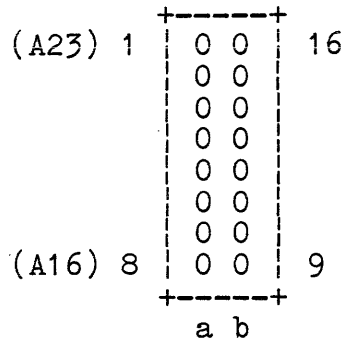
EXAMPLE:

To map the Data Packet Buffer into the last 2 Kbytes of the master's 1 Megabyte address range, install jumpers in positions corresponding to A20 through A23 and leave A11 through A19 open. Install a jumper in ENABLE EXTN ADDR. Note: The LANS100 is shipped per the configuration shown below.
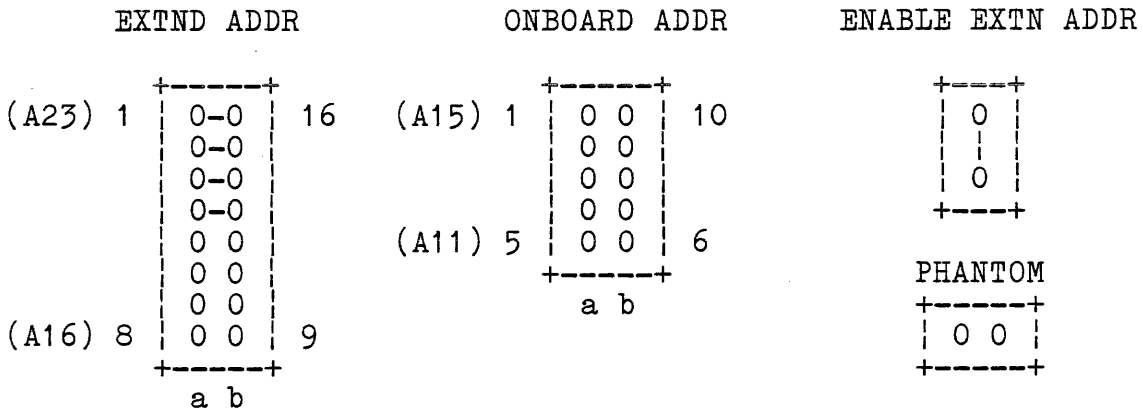
```
       EXTND ADDR                ONBOARD ADDR              ENABLE EXTN ADDR

                                                             +===+
  (A23) 1 | 0-0 | 16       (A15) 1 | 0  0 | 10               | 0 |
          | 0-0 |                  | 0  0 |                   | | |
          | 0-0 |                  | 0  0 |                   | 0 |
          | 0-0 |                  | 0  0 |                   +---+
          | 0  0 |          (A11) 5 | 0  0 | 6
          | 0  0 |                  +------+                  PHANTOM
          | 0  0 |                    a  b                   +------+
  (A16) 8 | 0  0 | 9                                         | 0  0 |
          +------+                                           +------+
            a  b
```

Note: 1. A jumper installed corresponds to a logic 0
           setting and the absence of a jumper
           corresponds to a logic 1 setting.

       2. Any other S100 Bus device installed in the bus
           that is memory mapped may not reside within
           the address space assigned to the LANS100.

ONBOARD ADDRESS (ONBOARD ADDR)

        During master memory access cycles in PHANTOM MODE, the
address lines A0 through A10 address one of 2 Kbytes of the Data
Packet Buffer whereby address lines A11 through A15 map the Data
Packet Buffer onto the master's address space but with PHANTOM
activated in order that the master's system memory does not
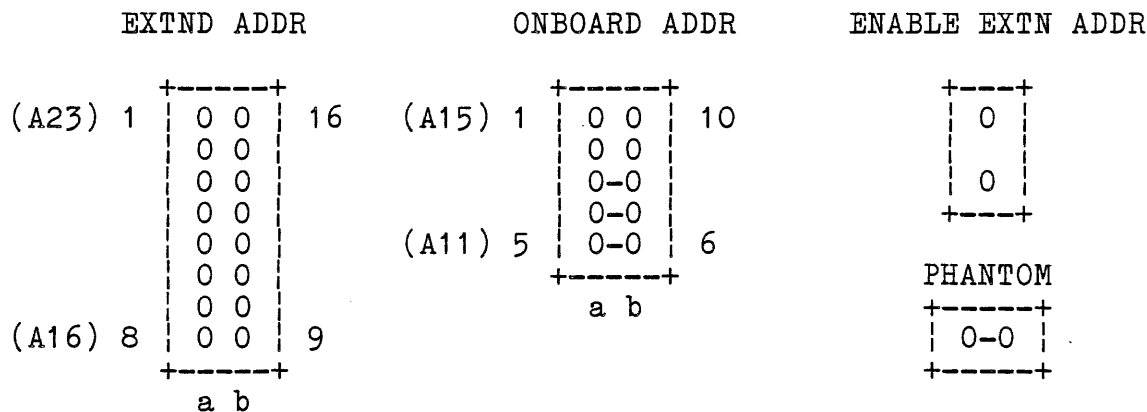conflict with the Data Packet Buffer. The ENABLE EXTN ADDR jumper
is not installed and only the ONBOARD ADDR jumper is configured
to specify the system's address space in which the Data Packet
Buffer is to appear. Thus, A11 through A15 are compared against
the ONBOARD ADDR jumper. The jumper PHANTOM must also be
installed.

EXAMPLE:

        To map the Data Packet Buffer into 2 Kbytes of the
        master's 64 Kbyte onboard   address range, at
        location C000, install jumpers in positions corres-
        pondingto A11, A12 and A13.   Leave A14and A15 open.
        Install a jumper in PHANTOM and remove the jumper in
        ENABLE EXTN ADDR.

          EXTND ADDR   ONBOARD ADDR   ENABLE EXTN ADDR

              +-----+   +-----+   +---+
    (A23) 1 | 0 0 | 16   (A15) 1 | 0 0 | 10 | 0 |
            | 0 0 | | 0 0 | | |
            | 0 0 | | 0-0 | | 0 |
            | 0 0 | | 0-0 | +---+
            | 0 0 | (A11) 5 | 0-0 | 6
            | 0 0 | +-----+   PHANTOM
            | 0 0 | a b   +-----+
    (A16) 8 | 0 0 | 9 | 0-0 |
            +-----+   +-----+
              a b

ENABLE EXTENDED ADDRESS (ENABLE EXTN ADDR)

When the master executes a memory access cycle in extended address mode, a comparator on the LANS100 is enabled which compares the master's extended address lines A16 through A23 against the eight position EXTND ADDR jumper. The remaining mapped address lines A11 through A15 are compared against the ONBOARD ADDR jumper. The EXTND ADDR jumper is sampled only if the ENABLE EXTN ADDR jumper is installed.

```
          EXTND ADDR
          +-----+
          | 0-0 |
          +-----+
```
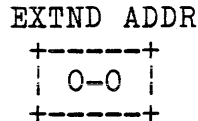
I/O PORT ADDRESS (IOPORT ADDR)

Address lines A0 through A7 are used by the LANS100 during master I/O cycles to transfer I/O commands from the master and status inputs to the master. The I/O Port Address Decoder consists of an eight bit comparator which compares the master's least significant address bits A0 through A7 against the eight position IOPORT ADDR jumper. If the master executes an I/O cycle transfer to the bus, and if the IOPORT ADDR jumper compares, the LANS100 will respond to either a master's command or to the master's request for the LANS100's status.

```
              IOPORT ADDR
              +-----+
      (A7) 1  | 0-0 | 16
              | 0 0 |
              | 0 0 |
              | 0-0 |
              | 0 0 |
              | 0-0 |
              | 0-0 |
      (A0) 8  | 0-0 | 9
              +-----+
               a b
```
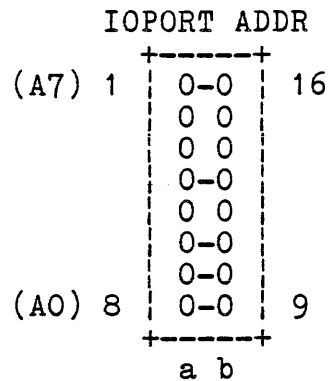
EXAMPLE:

To map the LANS100 into the I/O address space 68H, install a jumper in positions A0,A1,A2,A4 & A7 and none in the remaining positions. The LANS100 is shipped per the configuration as shown above.

Note: A jumper installed corresponds to a logic 0 setting and the absence of a jumper corresponds to a logic 1 setting.

LANS100 IDENTIFICATION (LANC ID)

     The LANC reads in a jumper settable identification code used for node identification purposes. A jumper setting is input to a shift register and the LANC reads the contents of the shift register during reset time. The jumper is identified on the board as LANC ID.

LANC ID

```
                +-----+
(MSB) 1 |  0  0  |  🔥
      2 |  0  0  |
      3 |  0  0  |
      4 |  0  0  |
      5 |  0  0  |
      6 |  0  0  |
      7 |  0  0  |
(LSB) 8 |  0  0  |  🔥
                +-----+
                 a  b
```
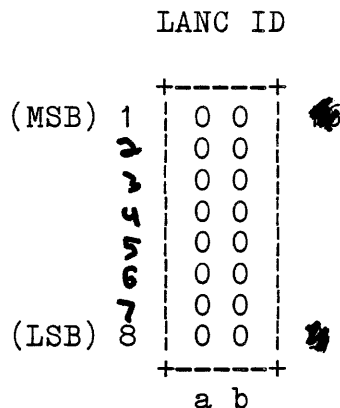

EXAMPLE:

     To configure the LANS100 identification number for F5 hex, install a jumper from a7 to b7.

Note: 1. A jumper installed corresponds to a logic 0 setting and the absence of a jumper corresponds to a logic 1 setting.

        2. Under no circumstances should 2 or more boards have the same ID settings while attached to the same coax bus structure. Each master system must have its own ID setting.

        3. ID setting 00 hex is not allowed as the COM9026 uses ID 00 as its global broadcast to all nodes attached to the network.

RESET SELECT

       The LANS100's reset line is asserted to clear the LANC
and other internal logic. One of three reset sources from the
master cause the LANS100 reset line to be asserted. The
selection of these reset signals is done via jumper option RESET
SELECT. The reset signals are:

    - Reset
    The master may issue a reset signal by asserting the bus
    reset signal RESET (S100 Bus pin 75).

    - Slave Clear
    The master may issue a reset signal by asserting the bus
    reset signal SLVCLR (S100 Bus pin 54). The LANS100 is
    shipped per the configuration as shown below.

    - Power-On Clear
    The master may issue a reset signal by asserting the bus
    reset signal POC (S100 Bus pin 99).

                        RESET SELECT

                           +---+
        Reset------------>|. 0 | 1
                           +---+ |
        Slvclr---->4 | 0---0 | 2
                           +---+ |
        POC-------------->| 0 | 3
                           +---+
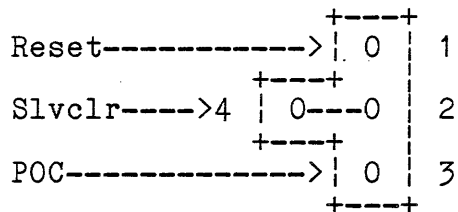
       To select RESET, connect from 1 to 2.
       To select SLAVE CLEAR, connect from 4 to 2.
       To select POWER-ON CLEAR, connect from 3 to 2.

READY SELECT

The LANS100 generates wait states to the host processor when the host processor executes either memory or I/O request cycles (MREQ or IORQ respectively). The user has the option to generate the wait states either through XRDY or PRDY by selecting the wait generator source to the appropriate S100 Bus pin (jumper- READY SELECT). The LANS100 is factory set to PRDY.

                         READY SELECT

                        +---+
                   1 | 0 |----> XRDY
                   2 | 0 |
                   3 | 0 |----> PRDY
                        +---+
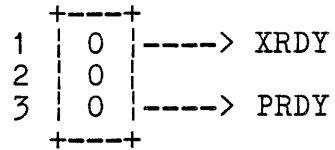
              Connect 1 to 2 to select XRDY.
              Connect 3 to 2 to select PRDY.

ENABLE
EXTENDED
ADDRESS

I/O PORT
ADDRESS

ONBOARD
ADDRESS

LAN CONTROLLER ID

SPARE U1 C1 C2 SPARE U3 C3 C4 C5 SPARE U6 C6 C7 J1 R1 C8

U2 U4 U5 LANC ID U8

LANS 100
REV. A

INTERCONTINENTAL MICRO SYSTEMS CORP.
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IO PORT ADDR

ONBOARD ADDR

VR1

C9

C10

C11 C12 16 1 10 1 C13 C14 C15 C16 MSB RP1 TOUT1 C17 LAND

U9

PHANTOM 1 ☐ 2 18 9 5 6 TOUT2

2 A0 RP2 RP3 U10 U11 U12 U13 C18 C19

ENABLE
EXTN ADDR C20

EXTND
ADDR

VR2 16 1 16 C24 C26 C27 C28 U14 U15

i 1 C23 C25 C29

3 RESET
READY SELEC
SELECT

8 9 8 9 RESET
VI SELEC
SELECT A16

SIXTN PU 1 ☐ 2 U16 U17 U18 U19 U20 U21 U22 U23 U24

C21 RP4

C22 1 P1 50

READY SELECT

EXTENDED
ADDRESS

RESET
SELECT

- FIGURE 1 -
JUMPER OPTIONS

SOLDER/TRACE CUT OPTIONS

Refer to figure 2 to locate the solder/trace cut areas. These are listed as follows:

    TOUT1
    TOUT2
    SIXTN PU
    PHANTOM
    VI SELECT

-----   -----
TOUT1   TOUT2
-----   -----

The TOUT1 and TOUT2 jumpers allow the network to operate over longer distances than 4 miles. The table below illustrates the Response Time and Reconfiguration time as a function of the TOUT1 and TOUT2 jumpers. The idle time will always be equal to the Response Time plus 3.5 microseconds. It should be noted that for proper network operation, all COM9026's connected to the same network must have the same response time, idle time and reconfiguration time. The LANS100 is factory set to a Response Time of 74.7 microseconds and Reconfiguration Time of 840 milliseconds.

TOUT2	TOUT1	RESPONSE TIME (US)	RECONFIGURATION TIME (MS)
1	1	74.7	840
1	0	283.4	1680
0	1	561.8	1680
0	0	1118.6	1680

Note: A jumper installed corresponds to a logic 0 setting and the absence of a jumper corresponds to a logic 1 setting.

SIXTN PU

The LANS100 is compatible with IEEE 16 data bit processors such as 8086 based Cpu's; however the LANS100 transfers 8 bit data only. In accordance with the IEEE 696.1/D2 specification, SIXTN is interrogated by the host to determine if the data bus transfer consists of 16 or 8 data bits. If SIXTN* is found to be at a logic high, the host transfers 8 data bits. The LANS100 must be strapped to present a logic high on the SIXTN* line. This is accomplished by providing a strap on SIXTN PU.
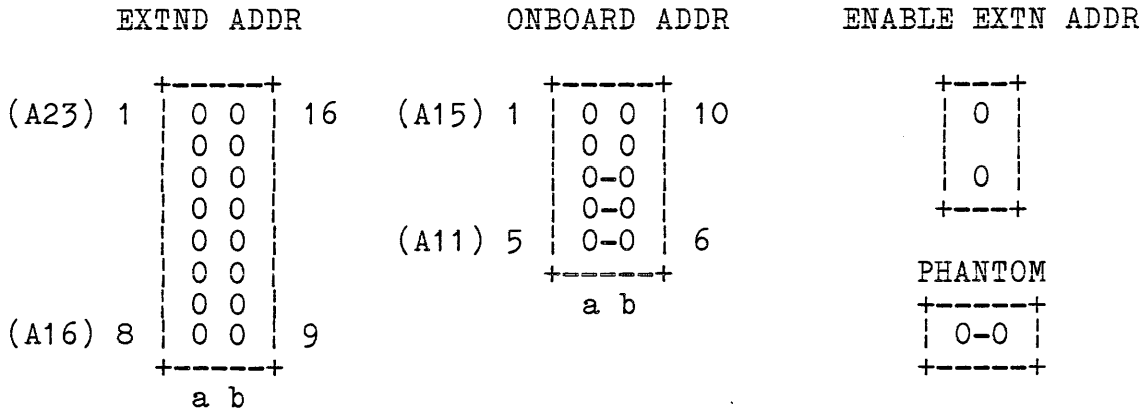
[SIXTN PU] area

```
+-+
|0|
|0|
+-+
```

PHANTOM

     During master memory access cycles in PHANTOM MODE, the
address lines A0 through A10 address one of 2 Kbytes of the Data
Packet Buffer whereby address lines A11 through A15 map the Data
Packet Buffer onto the master's address space but with PHANTOM
activated in order that the master's system memory does not
conflict with the Data Packet Buffer. The ENABLE EXTN ADDR jumper
is not installed and only the ONBOARD ADDR jumper is configured
to specify the system's address space in which the Data Packet
Buffer is to appear. Thus, A11 through A15 are compared against
the ONBOARD ADDR jumper. The jumper PHANTOM must also be
installed.

     EXAMPLE:

          To map the Data Packet Buffer into 2 Kbytes of the
          master's 64 Kbyte onboard address range, at
          location C000, install jumpers in positions corres-
          pondingto A11, A12 and A13. Leave A14and A15 open.
          Install a jumper in PHANTOM and remove the jumper in
          ENABLE EXTN ADDR.

```
        EXTND ADDR                 ONBOARD ADDR            ENABLE EXTN ADDR

         +-----+                    +-----+                   +---+
(A23) 1 | 0 0 | 16        (A15) 1 | 0 0 | 10                | 0 |
        | 0 0 |                    | 0 0 |                   |   |
        | 0 0 |                    | 0-0 |                   | 0 |
        | 0 0 |                    | 0-0 |                   +---+
        | 0 0 |           (A11) 5 | 0-0 | 6
        | 0 0 |                    +-----+                   PHANTOM
        | 0 0 |                      a b                     +-----+
(A16) 8 | 0 0 | 9                                            | 0-0 |
        +-----+                                              +-----+
          a b
```
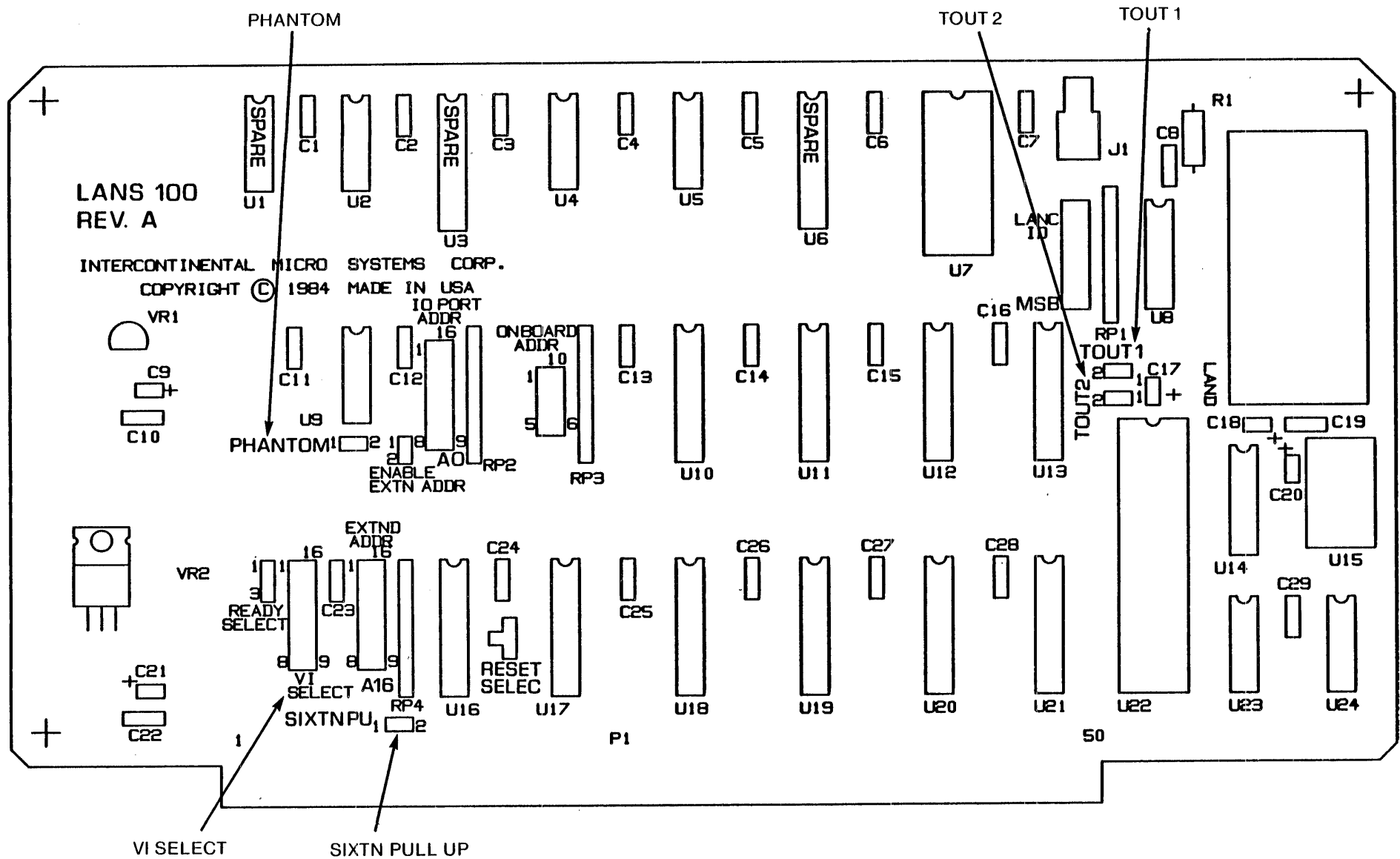

VI SELECT

     The LANS100 may assert an interrupt to the host (Vectored
Interrupt Request). The interrupt may be connected to one of 8 VI
lines of the S100 bus. This is accomplished by connecting a strap
on the VI SELECT jumper area.

[VI SELECT] area

```
    VIO                VI7
    +------------------+
  a| 0 0 0 0 0 0 0 0   |
  b| 0 0 0 0 0 0 0 0   |
    +------------------+
     1 2 3 4 5 6 7 8
```


     As an example, to connect Interrupt Request to VI1, connect
a jumper from a2-to-b2.

- FIGURE 2 -
SOLDER/TRACE CUT OPTIONS

**** SOFTWARE SECTION ****

This section describes the use of the LANS100 controller board with the TurboDOS operating system. This board provides the facilities for linking independent master systems, running Multiuser TurboDOS, together for common DATA, PRINTER, and SPOOLER operations between master sytems.

HARDWARE Configuration (LANS100 BOARD)

All LANS100 boards for all systems reside in the same memory space and I/O space address. Each board shipped from Intercontinental Micro Systems will be configured for their default Memory and I/O space address, so that the customer will not have to be concerned about it.

DEFAULT Address = FF800h (Last 2K of 1st 1 Megabyte ext. address)
DEFAULT I/O address = 68H

Each LANS100 board will also be shipped with the board ID jumpers already set. The ID jumpers establishes that board's network ID address so that during a power up, the entire network can establish who is attached to the network. Under no circumstances should 2 or more boards have the same ID switch settings while attached to the same coax bus structure. Each master system must have its own ID setting. NOTE: ID setting 00 is not allowed on any LANS100 board as this is the Internal Broadcast ID of the 9026 to all LANS100 boards attached to the system. The GLOBAL Broadcast function is not used by I.C.M.

ID Jumper Settings

_____

O = Open jumper position
S = Close jumper position

Position ---	1	2	3	4	5	6	7	8
ID	¦	¦	¦	¦	¦	¦	¦	¦
01	S	S	S	S	S	S	S	O
02	S	S	S	S	S	S	O	S
03	S	S	S	S	S	S	O	O
04	S	S	S	S	S	O	S	S
05	S	S	S	S	S	O	S	O
				etc				
FE	O	O	O	O	O	O	O	S
FF	O	O	O	O	O	O	O	O

SOFTWARE setup (LANS100 BOARD)

_____

   The LANS100 driver module (ACRNET.REL) as shipped from I.C.M.
does not have any GLOBAL patch points for GEN.COM to deal with,
as the ARCNET(LANS100) driver module is self configuring to the
system.

   Below is an example .GEN and .PAR file for implementing the
LANS100 driver into 2 systems known as SYSTEM A: and SYSTEM B:.

Intercontinental Micro Systems, Corp.
TurboDOS V1.3 System Example

SYSTEM A:
T O P O L O G Y

         Name   Assignment
         Master .... Printer "A"
         Slave-1 .... Printer "B"
         Slave-2 .... Printer "C"
         Slave-3 .... Printer (none)
         Remote Printer A (system B) ... Printer "D"
         Remote Drive A (system B) ..... Drive "C"
         Remote Drive B (system B) ..... Drive "D"

                        N O T E :
         LANS100 Board ID = 01 in this System.

         CPZMASTR.GEN file

STDMASTR   ; Standard networking master
FASLOD   ; Use fast disk loader module
MSGFMT   ; Delete if not SPOOLING with SLAVES
NETREQ   ; Delete if not SPOOLING with SLAVES
CPMSUP   ; CP/M function support module
CONREM   ; Use remote console module
;CON192   ; Null 19.2 Kbaud Console Driver
;CON96   ; Null 9600 Baud Console driver
CPZBRT   ; CPZ-4800X baud rate and RTC constants
CPZDINIT   ; CPZ-4800X driver initialization
CPZNIT   ; CPZ-4800X hardware initialization
CPZIO   ; CPZ-4800X Serial and Parallel I/O
LSTCTS   ; TI810 CTS Driver (LSTDR@ assigned to LSTDRA)
;LSTPAR   ; Centronics Parallel port printer
CPZRTC   ; CPZ-4800X real time clock driver
MSTRCLK   ; ICM clk board drvr to set TurboDOS date/time
CPZFDC   ; CPZ-4800X floppy disk driver
DSKFMT8   ; Disk specification tables for 8-INCH diskettes
;MD131DRV   ; Monitor Dynamics Model #1013 with 1 drive
;MD132DRV   ; Monitor Dynamics Model #1013 with 2 drive
;TURBO   ; Turbo-Disk driver module
;TURDSK   ; Turbo-Disk definition module
CPZMCD   ; CPZ-4800X / CPS-MX Master Circuit Driver
LANS100   ; Include LANS100 Driver module

CPZMASTR.PAR file

```
SRHDRV = OFF                    ; Search system disk for command files
COMPAT = OF8                    ; Record/File lock compatibility flags
;
NMBUFS = OA                     ; Default number of Disk Buffers (hex)
BUFSIZ = 03                     ; Default disk buff size (log2(size/128))
MEMRES = (0400)                 ; Reserve memory for dynamic allocations
;
NMBCKT = 2                      ; Define the number of circuit drivers
CKTAST = (0000),CKTDRA,(0100),CKTDRB ; Slaves, ARCNET circuits
;
NMBCPS = 03                     ; Number of CPS-MX slaves supported
NMBSVC = 04                     ; Nmb. of "server processes" (slvs & ARC)
NMBMBS = OC                     ; Pre-allocate NMBSVC * 3 message buffers
NMBRPS = OC                     ; Pre-allocate NMBSVC * 3 reply buffers
;
CKTCPS = 00                     ; CPS-MX network circuit number
PATCPS = 7F,7E,7D,7C            ; Status port table for CPS-MX
MPTCPS = 01                     ; Memory page table for CPS-MX
SSTCPS = "123"                  ; O/S suffix table for CPS-MX
;
AUTUSR = 80                     ; Auto Log-on to user one, privileged
;
PTRAST = 00,LSTDRA,81,(1),82,(2) ; List assignment TABLE
         80,(0102)                      ; Remote Printer A = local "D"
QUEAST = 00,(0),81,(1),82,(2)    ; Queue assignment TABLE
         80,(0102)                   ; Remote Queue A = local QUEUE "D"
DSPPAT = 1,2,3,4                ; 4 printers
;
FLSRT  = 01                     ; 6ms Floppy step rate
ATNCHR = "^@"                   ; New attention character
;
;MPAGE = 02        ; Use memory above slave address for Turbo-disk
;
;following defines floppy disk drives
;
DSKAST = 000,DSKDRA,001,DSKDRA        ; Local Floppys A:, B:
         080,(0102),081,(0102)         ; Remote A:& B:= local C: & D:
;
```

Slave-1 GEN file

```
STDSLAVE            ; Standard NETWORKING SLAVE
BNKMGR             ; ONLY If using BANKED 128K Slave.
;NETLOD            ; Usenetworkload module (ifnotbanked slave)
NETSVC             ; Include Net service module
RTCNUL             ; allow consistant printing with de-spooler
DSPOOL             ; include de-spool module
CPMSUP             ; CP/M Function support module
CPSDINIT           ; CPS-MX Driver Initialization
CPSNIT             ; CPS-MX hardware initialization
CON192             ; 19.2K baud console Driver
;CON96             ; 9600 baud console Driver
CPSIO              ; CPS-MX Serial Drivers
LSTCTS             ; Use list clear to send null driver
;LSTPAR            ; Use parallel null driver
CPSSCD             ; CPS-MX Slave Circuit driver
CPSRES             ; CPS-MX Slave reset detection
;-------------------------------------------------------------------
```
Slave-1 PAR file

```
SRHDRV = OFF       ; Search System Disk for .COM Files
COMPAT = OF8       ; File/Record Locking Compatibility Flags
;
;CPMVER = 022      ; Inhibit CB-80 Record Locking
;
ATNCHR = "^@"      ; Use "BREAK" Key for Attention
RESKEY = "^\"      ; Reset key function
AUTUSR = 80        ; DEFAULT = User 0, Privileged
;
CURBNK = 1         ; Default bank = TPA if 1 (and banked slave)
NMBMBS = 2         ; Pre-Allocate NMBCKT Msg Buffers (Simple Slave)
NMBRPS = 2         ; Pre-Allocate NMBCKT Reply Waiting
                   ; Packets (Simple Slave)
;
CONAST = 01,CONDRA     ; Console on port 1 of CPS-MX
STOPBB = 44            ; define 1 stop bit on console
STOPBA = 44            ; define 1 stop bits on printer
;
PTRAST+3 = 00,LSTDRA   ;1 local, rest remote printers
QUEAST+3 = 00,(0)      ;1 local, rest remote queues
DSPPAT = 1,2,3,4       ; assign printers
QUEPTR = 2             ; assign as printer A
PRTMOD = 1             ;1=spooled, 0=direct
;
LDCOLD = 000       ; Disable Cold start autoload
LDWARM = 000       ; Disable Warm start autoload
;
;LDCOLD must be set to OFF if you want to auto-load a file
;
;COLDFN = 0,"SLVCLK  ","AUT"     ;init system clock function using
                                 ;CCB-100 clock board.
```

Slave-2 GEN file

```
STDSLAVE            ; Standard NETWORKING SLAVE
BNKMGR              ; ONLY If using BANKED 128K Slave.
;NETLOD             ; Usenetworkload module (ifnotbanked slave)
NETSVC              ; Include Net service module
RTCNUL             ; allow consistant printing with de-spooler
DSPOOL             ; include de-spool module
CPMSUP             ; CP/M Function support module
CPSDINIT           ; CPS-MX Driver Initialization
CPSNIT             ; CPS-MX hardware initialization
CON192             ; 19.2K baud console Driver
;CON96             ; 9600 baud console Driver
CPSIO              ; CPS-MX Serial Drivers
LSTCTS             ; Use list clear to send null driver
;LSTPAR            ; Use parallel null driver
CPSSCD             ; CPS-MX Slave Circuit driver
CPSRES             ; CPS-MX Slave reset detection
;--------------------------------------------------------------
```

Slave-2 PAR file

```
SRHDRV = OFF        ; Search System Disk for .COM Files
COMPAT = OF8        ; File/Record Locking Compatibility Flags
;
;CPMVER = 022       ; Inhibit CB-80 Record Locking
;
ATNCHR = "^@"       ; Use "BREAK" Key for Attention
RESKEY = "^\"       ; Reset key function
AUTUSR = 80         ; DEFAULT = User 0, Privileged
;
CURBNK = 1          ; Default bank = TPA if 1 (and banked slave)
NMBMBS = 2          ; Pre-Allocate NMBCKT Msg Buffers (Simple Slave)
NMBRPS = 2          ; Pre-Allocate NMBCKT Reply Waiting
                    ; Packets (Simple Slave)
;
CONAST = 01,CONDRA       ; Console on port 1 of CPS-MX
STOPBB = 44              ; define 1 stop bit on console
STOPBA = 44              ; define 1 stop bits on printer
;
PTRAST+6 = 00,LSTDRA     ;2 remote, 1 local printer
QUEAST+6 = 00,(0)        ;2 remote, 1 local queue
DSPPAT = 1,2,3,4         ;assign number of printers
QUEPTR = 3               ;assign this printer as "C"
PRTMOD = 1               ;1=spooled, 0=direct
;
LDCOLD = 000        ; Disable Cold start autoload
LDWARM = 000        ; Disable Warm start autoload
;
;LDCOLD must be set to OFF if you want to auto-load a file
;
;COLDFN = 0,"SLVCLK  ","AUT"      ;init system clock function using
                                  ;CCB-100 clock board.
;--------------------------------------------------------------
```

Slave-3 GEN file

```
STDSLAVE          ; Standard NETWORKING SLAVE
BNKMGR            ; ONLY If using BANKED 128K Slave.
;NETLOD           ; Usenetworkload module (ifnotbanked slave)
NETSVC            ; Include Net service module
RTCNUL            ; allow consistant printing with de-spooler
CPMSUP            ; CP/M Function support module
CPSDINIT          ; CPS-MX Driver Initialization
CPSNIT            ; CPS-MX hardware initialization
CON192            ; 19.2K baud console Driver
;CON96            ; 9600 baud console Driver
CPSIO             ; CPS-MX Serial Drivers
;LSTCTS           ; Use list clear to send null driver
;LSTPAR           ; Use parallel null driver
CPSSCD            ; CPS-MX Slave Circuit driver
CPSRES            ; CPS-MX Slave reset detection
;----------------------------------------------------------------
```
Slave-3 PAR file

```
SRHDRV = OFF      ; Search System Disk for .COM Files
COMPAT = OF8      ; File/Record Locking Compatibility Flags
;
;CPMVER = 022     ; Inhibit CB-80 Record Locking
;
ATNCHR = "^@"     ; Use "BREAK" Key for Attention
RESKEY = "^\"     ; Reset key function
AUTUSR = 80       ; DEFAULT = User 0, Privileged
;
CURBNK = 1        ; Default bank = TPA if 1 (and banked slave)
NMBMBS = 2        ; Pre-Allocate NMBCKT Msg Buffers (Simple Slave)
NMBRPS = 2        ; Pre-Allocate NMBCKT Reply Waiting
                  ; Packets (Simple Slave)
;
CONAST = 01,CONDRA     ; Console on port 1 of CPS-MX
STOPBB = 44            ; define 1 stop bit on console
;
LDCOLD = 000      ; Disable Cold start autoload
LDWARM = 000      ; Disable Warm start autoload
;
;LDCOLD must be set to OFF if you want to auto-load a file
;
;COLDFN = 0,"SLVCLK  ","AUT"     ;init system clock function using
                                 ;CCB-100 clock board.
;----------------------------------------------------------------
```

Intercontinental Micro Systems, Corp.
TurboDOS V1.3 System Example

SYSTEM B:
T O P O L O G Y
————————————

```
          Name                              Assignment
          Master ........................ Printer "A"
          Slave-1 ....................... Printer "B"
          Slave-2 ....................... Printer "C"
          Slave-3 ....................... Printer (none)
          Remote Printer A (system A) ... Printer "D"
          Remote Drive A (system A) ..... Drive "E"
          Remote Drive B (system A) ..... Drive "F"


                     N O T E :
          LANS100 Board ID = 02 in this System.
```

          CPZMASTR.GEN file

```
STDMASTR            ; Standard networking master
FASLOD              ; Use fast disk loader module
MSGFMT              ; Delete if not SPOOLING with SLAVES
NETREQ              ; Delete if not SPOOLING with SLAVES
CPMSUP              ; CP/M function support module
CONREM              ; Use remote console module
;CON192             ; Null 19.2 Kbaud Console Driver
;CON96              ; Null 9600 Baud Console driver
CPZBRT              ; CPZ-4800X baud rate and RTC constants
CPZDINIT            ; CPZ-4800X driver initialization
CPZNIT              ; CPZ-4800X hardware initialization
CPZIO               ; CPZ-4800X Serial and Parallel I/O
LSTCTS              ; TI810 CTS Driver (LSTDR@ assigned to LSTDRA)
;LSTPAR             ; Centronics Parallel port printer
CPZRTC              ; CPZ-4800X real time clock driver
MSTRCLK             ; ICM clk board drvr to set TurboDOS date/time
CPZFDC              ; CPZ-4800X floppy disk driver
DSKFMT8             ; Disk specification tables for 8-INCH diskettes
;MD131DRV           ; Monitor Dynamics Model #1013 with 1 drive
;MD132DRV           ; Monitor Dynamics Model #1013 with 2 drive
;TURBO              ; Turbo-Disk driver module
;TURDSK             ; Turbo-Disk definition module
CPZMCD              ; CPZ-4800X / CPS-MX Master Circuit Driver
LANS100             ; Include LANS100 Driver module
```

CPZMASTR.PAR file

```
SRHDRV = OFF                    ; Search system disk for command files
COMPAT = OF8                    ; Record/File lock compatibility flags
;
NMBUFS = OA                     ; Default number of Disk Buffers (hex)
BUFSIZ = 03                     ; Default disk buff size (log2(size/128))
MEMRES = (0400)                 ; Reserve memory for dynamic allocations
;
NMBCKT = 2                      ; Define the number of circuit drivers
CKTAST = (0000),CKTDRA,(0100),CKTDRB ; Slaves, ARCNET circuits
;
NMBCPS = 03                     ; Number of CPS-MX slaves supported
NMBSVC = 04                     ; Nmb. of "server processes" (slvs & ARC)
NMBMBS = OC                     ; Pre-allocate NMBSVC * 3 message buffers
NMBRPS = OC                     ; Pre-allocate NMBSVC * 3 reply buffers
;
CKTCPS = 00                     ; CPS-MX network circuit number
PATCPS = 7F,7E,7D,7C            ; Status port table for CPS-MX
MPTCPS = 01                     ; Memory page table for CPS-MX
SSTCPS = "123"                  ; O/S suffix table for CPS-MX
;
AUTUSR = 80                     ; Auto Log-on to user one, privileged
;
PTRAST = 00,LSTDRA,81,(1),82,(2) ; List assignment TABLE
         80,(0101)                  ; Remote Printer A = local "D"
QUEAST = 00,(0),81,(1),82,(2)      ; Queue assignment TABLE
         80,(0101)                  ; Remote Queue A = local QUEUE "D"
DSPPAT = 1,2,3,4                   ; 4 printers
;
FLSRT  = 01                     ; 6ms Floppy step rate
ATNCHR = "^@"                   ; New attention character
;
;MPAGE = 02        ; Use memory above slave address for Turbo-disk
;
;following defines floppy disk drives
;
DSKAST = 000,DSKDRA,001,DSKDRA        ; Local Floppys A:, B:
         OFF,(0000),OFF,(0000)    ;  Un-Defined drives C: & D:
         080,(0101),081,(0101)     ; Remote A:& B:= local E: & F:
;
```

Slave-1 GEN file

```
STDSLAVE        ; Standard NETWORKING SLAVE
BNKMGR          ; ONLY If using BANKED 128K Slave.
;NETLOD         ; Usenetworkload module (ifnotbanked slave)
NETSVC          ; Include Net service module
RTCNUL          ; allow consistant printing with de-spooler
DSPOOL          ; include de-spool module
CPMSUP          ; CP/M Function support module
CPSDINIT        ; CPS-MX Driver Initialization
CPSNIT          ; CPS-MX hardware initialization
CON192          ; 19.2K baud console Driver
;CON96          ; 9600 baud console Driver
CPSIO           ; CPS-MX Serial Drivers
LSTCTS          ; Use list clear to send null driver
;LSTPAR         ; Use parallel null driver
CPSSCD          ; CPS-MX Slave Circuit driver
CPSRES          ; CPS-MX Slave reset detection
;-----------------------------------------------------------
```

Slave-1 PAR file

```
SRHDRV = OFF         ; Search System Disk for .COM Files
COMPAT = OF8         ; File/Record Locking Compatibility Flags
;
;CPMVER = 022        ; Inhibit CB-80 Record Locking
;
ATNCHR = "^@"        ; Use "BREAK" Key for Attention
RESKEY = "^\"        ; Reset key function
AUTUSR = 80          ; DEFAULT = User 0, Privileged
;
CURBNK = 1           ; Default bank = TPA if 1 (and banked slave)
NMBMBS = 2           ; Pre-Allocate NMBCKT Msg Buffers (Simple Slave)
NMBRPS = 2           ; Pre-Allocate NMBCKT Reply Waiting
                     ; Packets (Simple Slave)
;
CONAST = 01,CONDRA       ; Console on port 1 of CPS-MX
STOPBB = 44              ; define 1 stop bit on console
STOPBA = 44              ; define 1 stop bits on printer
;
PTRAST+3 = 00,LSTDRA     ;1 local, rest remote printers
QUEAST+3 = 00,(0)        ;1 local, rest remote queues
DSPPAT = 1,2,3,4         ; assign printers
QUEPTR = 2               ; assign as printer A
PRTMOD = 1               ;1=spooled, 0=direct
;
LDCOLD = 000         ; Disable Cold start autoload
LDWARM = 000         ; Disable Warm start autoload
;
;LDCOLD must be set to OFF if you want to auto-load a file
;
;COLDFN = 0,"SLVCLK  ","AUT"    ;init system clock function using
                                ;CCB-100 clock board.
```

Slave-2 GEN file

```
STDSLAVE        ; Standard NETWORKING SLAVE
BNKMGR          ; ONLY If using BANKED 128K Slave.
;NETLOD         ; Usenetworkload module (ifnotbanked slave)
NETSVC          ; Include Net service module
RTCNUL          ; allow consistant printing with de-spooler
DSPOOL          ; include de-spool module
CPMSUP          ; CP/M Function support module
CPSDINIT        ; CPS-MX Driver Initialization
CPSNIT          ; CPS-MX hardware initialization
CON192          ; 19.2K baud console Driver
;CON96          ; 9600 baud console Driver
CPSIO           ; CPS-MX Serial Drivers
LSTCTS          ; Use list clear to send null driver
;LSTPAR         ; Use parallel null driver
CPSSCD          ; CPS-MX Slave Circuit driver
CPSRES          ; CPS-MX Slave reset detection
;-------------------------------------------------------------------
```

Slave-2 PAR file

```
SRHDRV = OFF     ; Search System Disk for .COM Files
COMPAT = OF8     ; File/Record Locking Compatibility Flags
;
;CPMVER = 022    ; Inhibit CB-80 Record Locking
;
ATNCHR = "^@"    ; Use "BREAK" Key for Attention
RESKEY = "^\"    ; Reset key function
AUTUSR = 80      ; DEFAULT = User 0, Privileged
;
CURBNK = 1       ; Default bank = TPA if 1 (and banked slave)
NMBMBS = 2       ; Pre-Allocate NMBCKT Msg Buffers (Simple Slave)
NMBRPS = 2       ; Pre-Allocate NMBCKT Reply Waiting
                 ; Packets (Simple Slave)
;
CONAST = 01,CONDRA      ; Console on port 1 of CPS-MX
STOPBB = 44             ; define 1 stop bit on console
STOPBA = 44             ; define 1 stop bits on printer
;
PTRAST+6 = 00,LSTDRA    ;2 remote, 1 local printer
QUEAST+6 = 00,(0)       ;2 remote, 1 local queue
DSPPAT = 1,2,3,4        ;assign number of printers
QUEPTR = 3              ;assign this printer as "C"
PRTMOD = 1              ;1=spooled, 0=direct
;
LDCOLD = 000     ; Disable Cold start autoload
LDWARM = 000     ; Disable Warm start autoload
;
;LDCOLD must be set to OFF if you want to auto-load a file
;
;COLDFN = 0,"SLVCLK  ","AUT"       ;init system clock function using
                                   ;CCB-100 clock board.
;-------------------------------------------------------------------
```

Slave-3 GEN file

```
STDSLAVE            ; Standard NETWORKING SLAVE
BNKMGR             ; ONLY If using BANKED 128K Slave.
;NETLOD            ; Usenetworkload module (ifnotbanked slave)
NETSVC             ; Include Net service module
RTCNUL             ; allow consistant printing with de-spooler
CPMSUP             ; CP/M Function support module
CPSDINIT           ; CPS-MX Driver Initialization
CPSNIT             ; CPS-MX hardware initialization
CON192             ; 19.2K baud console Driver
;CON96             ; 9600 baud console Driver
CPSIO              ; CPS-MX Serial Drivers
;LSTCTS            ; Use list clear to send null driver
;LSTPAR            ; Use parallel null driver
CPSSCD             ; CPS-MX Slave Circuit driver
CPSRES             ; CPS-MX Slave reset detection
;----------------------------------------------------------------
```

Slave-3 PAR file

```
SRHDRV = OFF       ; Search System Disk for .COM Files
COMPAT = OF8       ; File/Record Locking Compatibility Flags
;
;CPMVER = 022      ; Inhibit CB-80 Record Locking
;
ATNCHR = "^@"      ; Use "BREAK" Key for Attention
RESKEY = "^\"      ; Reset key function
AUTUSR = 80        ; DEFAULT = User 0, Privileged
;
CURBNK = 1         ; Default bank = TPA if 1 (and banked slave)
NMBMBS = 2         ; Pre-Allocate NMBCKT Msg Buffers (Simple Slave)
NMBRPS = 2         ; Pre-Allocate NMBCKT Reply Waiting
                   ; Packets (Simple Slave)
;
CONAST = 01,CONDRA      ; Console on port 1 of CPS-MX
STOPBB = 44             ; define 1 stop bit on console
;
LDCOLD = 000       ; Disable Cold start autoload
LDWARM = 000       ; Disable Warm start autoload
;
;LDCOLD must be set to OFF if you want to auto-load a file
;
;COLDFN = 0,"SLVCLK  ","AUT"      ;init system clock function using
                                  ;CCB-100 clock board.
;----------------------------------------------------------------
```

All products sold hereunder are under warranty on a return to factory basis against defects in workmanship and material for a period of one (1) year from the date of delivery.

Conditions of this warranty are as follows: Purchaser must 1) obtain a return material authorization (RMA) number and shipping instructions, 2) product must be shipped prepaid, 3) written description of the failure must be included with the defective product. All transportation charges inside the continental U.S. will be paid by Intercontinental Micro Systems (ICM) Corp. For products returned from all other locations, transportation must be prepaid. Should ICM determine that the products are not defective, the purchaser must pay all return transportation charges. All repairs will be provided at repair rates being charged at the time by ICM. Under the above product warranty, ICM may, at its option, either repair or replace any component which fails during the warranty period providing the purchaser has reported same in a prompt manner. All replaced products or parts shall become property of ICM.

All above warranties are contingent upon proper use of the product. These warranties will not apply 1) if any repair, parts replacement, or adjustments are necessary due to accident , unusual physical, electrical or electromagnetic stress, neglect, misuse, failure of electric power, air conditioning, humidity control, transportation, failure of rotating media not furnished by ICM, operation with media not meeting or not maintained in accordance with ICM specifications or causes other than ordinary use, 2) if the product has been modified by purchaser, 3) where ICM's serial numbers or warranty date decals have been removed or altered, 4) if the product has been dismantled by purchaser without the supervision of or prior written approval of ICM.

EXCEPT FOR THE EXPRESS WARRANTIES CONTAINED HEREIN, ICM DISCLAIMS ALL WARRANTIES ON THE PRODUCTS FURNISHED HEREUNDER, INCLUDING ALL IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS; and the stated express warranties are in lieu of all obligations or liabilities on the part of ICM arising out of or in connection with the performance of the products. ICM is not liable for any indirect or consequential damages.

After the warranty period, the products will be repaired for a service charge plus parts, provided that it is returned prepaid to ICM after retaining a return material authorization (RMA) number.

ICM

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